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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,943	09/01/2000	Seung Kuk Ahn	8733-294-00	7898

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MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
KOVALICK, VINCENT E	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,943	AHN, SEUNG KUK	
	Examiner	Art Unit	
	Vincent E. Kovalick	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 10-17* is/are rejected.

7)☒ Claim(s) *7-9 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's Response to Non-Final Office Action dated August 2, 2006, in response to USPTO Office Action dated May 2, 2006.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 4-5, 11 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirakata (USP 6,496,172) taken with Hirakata et al. (USP 5,847,687).

Relative to claims 1, 5, 11 and 16, Hirakata ('172) **teaches** a liquid crystal display device, active matrix type liquid crystal display device, and method of driving the same (col. 5, lines 41-67; col. 6, lines 1-67 and col. 7, lines 1-16); Hirakata ('172) further **teaches** an apparatus and method for driving a liquid crystal panel having pixels arranged at each intersection between gate lines and data lines in a matrix type in an inversion system, comprising: first signal supplying means for setting at least one pixel block each of which includes at least two data lines within the liquid crystal panel to apply data signals having the same polarity to adjacent pixels in a gate line direction within the at least one pixel block (Fig. 17A).

Hirakata ('172) **does not teach a** second signal supplying means for applying data signals to pixels outside the at least one pixel block, wherein the applied data signals have a polarity

contrary to data signals applied to pixels adjacently arranged at left and right sides thereof and also arranged outside the at least one pixel block.

Hirakata et al. ('687) **teaches** a driving method of active matrix display device (col. 3, lines 35-67 and col. 4, lines 1-19); Hirakata et al. ('687) further **teaches a** second signal supplying means for applying data signals to pixels outside the at least one pixel block, wherein the applied data signals have a polarity contrary to data signals applied to pixels adjacently arranged at left and right sides thereof and also arranged outside the at least one pixel block (col. 6, lines 25-38 and Figs. 12A and 12B).

It would have been obvious to a person of ordinary skill in the a art at the time of the invention to provide to the device as taught by Hirakata (172) the feature as taught by Hirakata ('687) in order to reduce the operating voltage of the display device.

Regarding claim 2, Hirakata ('172) further **teaches** driving a liquid crystal panel wherein the pixel block is positioned at a boundary portion between column drivers (col. 16, lines 54-59 and Fig. 17A)

Regarding claim 3, Hirakata ('172) further **teaches** driving a liquid crystal panel wherein the pixel block includes at least two data lines to which a data is applied from the same column driver (Fig. 5, item 505).

Relative to claims 4 and 15, Hirakata ('172) further **teaches** driving a liquid crystal panel wherein all the pixels within the liquid crystal panel responds to the data signals having a polarity inverted every frame (col. 3, lines 22-25).

4. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirakata (172) taken with Hirakata ('687) as applied to claims 5 and 16 respectively in item 3 hereinabove, and further in view of Okumura et al. (USP 5,739,804).

Regarding claims 6 and 17, Hirakata ('172) taken with Hirakata ('687) **does not teach** a liquid crystal panel comprising line-inversion control means for controlling the first signal supplying means to apply the data signals having the same polarity to the adjacent pixels in the gate line direction; and dot-inversion control means for controlling the second signal supplying means to apply the data signals having a polarity contrary to the pixels at the left and right sides thereof. Hirakata teaches a liquid crystal display device with no flicker and with a bright display by using a frame inversion driving technique.

Okumura et al. **teaches** a liquid crystal display device in which a period other than an image display prior is extended (col. 7, lines 15-67 and col. 8, lines 1-65); Okumura et al. further **teaches** a liquid crystal panel comprising line-inversion control means for controlling the first signal supplying means to apply the data signals having the same polarity to the adjacent pixels in the gate line direction; and dot-inversion control means for controlling the second signal supplying means to apply the data signals having a polarity contrary to the pixels at the left and right sides thereof (col. 1, lines 53-62).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Hirakata ('172) taken with Hirakata ('687) the feature as taught by Okumura et al. in order to optimize the drive device output.

5. Claims 10, 12, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirakata ('172) taken with Hirakata ('687) as applied to claims 2 and 11 respectively in item 3 hereinabove, and further in view of Jeong et al. (USP 6,271,816).

Regarding claims 10 and 13, Hirakata ('172) taken with Hirakata ('687) **does not teach** a method wherein data lines within a least one first plurality of consecutively arranged data lines are connected to adjacent column drivers.

Jeong **teaches** a power saving circuit and method for driving an active matrix display (col. 3, lines 62-67 and col. 4, lines 1-7); Jeong et al. further **teaches teach** a method wherein data lines within a least one first plurality of consecutively arranged data lines are connected to adjacent column drivers (col. 2, lines 60-67; col. 5, lines 10-23 and col. 6, lines 49-62).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Hirak172) taken with Hirakata ('687) the feature as taught by Jeong et al. in order to provide the means to significantly reduce the power needed by the column drive circuit to drive voltages of alternating polarity onto the column electrodes , in this way significant power is saved in both the pixel inversion and the row inversion schemes (Jeong et al. col. 3, lines 66-67 and col. 4, lines 1-3).

Relative to claims 12 and 14, Jeong et al. further **teaches** the method step of providing a plurality of column drivers for applying the video signal, wherein each column driver is connected to a plurality of consecutively arranged data lines (col. 4, lines 65-67; col. 5, lines 1-9 and Fig. 1A).

Allowable Subject Matter

6. Claims 7-9 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Regarding claims 7 and 18, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** an apparatus for driving a liquid crystal panel wherein the first and second signal supplying means comprises at least two signal inverters for responding to control signals applied from the line inversion control means and the dot-inversion control means to invert phases of input data signals.

Response to Applicant's Remarks

8. Applicant's arguments filed August 2, 2006 have been fully considered but they are not persuasive.

Relative to claims 1 and 5 Applicant argues tha6 prior art Hirakata '172 does not teach "allowing pixels outside the at least one pixel block to respond to data signals having a polarity contrary to pixels adjacently arranged at left and right side thereof". Based on the language of the claim Hirakata '172 teaches in Figs. 17A and 17B a six column matrix divided into three blocks; columns 1-2 , and 3-4 and 5-6 each constitute a two column block respectively. Blocks 1 and 3 contain pixels that have responded to data signals having a polarity contrary to pixels in block 2, blocks 1 and 3 being adjacently arranged at left and right side and outside of block 2; as illustrated in Polarity Patterns (1) and (2) of Figs. 17A and 17B.

Regading Applicant's argument relative to claims 11, 15 and 16, wherein "applying video signals to at least one second plurality of consecutively arranged data lines such that video signals having opposite polarities are applied to pixels adjacent each other along a gate line direction". Hirakata '687 teaches in Figs. 12A and 12B and col. 6, lines 32-38, pixels adjacent to each other, along a gate line direction, maintaining data signals of opposite polarity.

It being understood that a first and second signal supply means would have to be in place in order to set the polarities as taught in claims 1, 5, 11, 15 and 16.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,559,822	Okuzono
U. S. Patent No.	6,400,350	Nishimura et al.
U. S. Patent No.	6,327,008	Fujiyoshi

Final Rejection

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

To Respond

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Vincent E. Kovalick
September 13, 2006